REMARKS

Introduction

This Reply is in response to the Office Action of January 11, 2005. Reconsideration of this application in view of the following remarks is respectfully requested.

This application was filed with 32 claims. In the Office Action, claims 6-10 and 19-26 were allowed. Claims 5, 12, 17, and 28 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form. In the present Reply, claims 12, 17, and 28 have not been rewritten in independent form because applicant is demonstrating that the independent claims from which claims 12, 17, and 28 depend are allowable. However, applicants reserve the right to pursue the allowed subject matter of claims 12, 17, and 28 during future prosecution should the present Reply not be considered to place the claims in condition for allowance.

Claims 1-4, 11, 13-16, 18, 27, and 29-32 were rejected under 35 U.S.C. §102(b) as being anticipated by Gabara U.S. Patent No. 5,977,796 ("Gabara"). These rejections are respectfully traversed.

Formal Drawings

Formal drawings are being submitted herewith to replace the informal drawings originally-filed with this patent application. The formal drawings comply with 37 1.121(d) and overcome the objections to the drawings raised in the Office Action.

Claim 1

In the Office Action, claim 5 was objected to as being dependent on a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. This has been done by amending claim 1 to incorporate the features of claim 5, which previously depended on claim 1. Claim 1 is therefore in condition for allowance.

Claims 2 and 4

Applicants' invention relates to dynamically-adjustable differential output drivers. Both the peak-to-peak output voltage swing V_{OD} and the common mode voltage V_{CM} of the differential output drivers can be adjusted to accommodate different system environments.

A differential output driver 46 in accordance with the invention is shown in FIG. 5 of applicants' specification. As

shown in FIG. 5, adjustable differential output driver 46 has adjustable output resistors 80, adjustable current sources 78, and an adjustable common-mode voltage source 86. As described at page 31, lines 13-21, current sources 78 may be adjusted via control terminals 82. Resistors 80 may be adjusted via control terminals 84. The level of the output voltage supplied by source 86 may be controlled using control input 88.

In a typical scenario, the resistance of resistors 80 is adjusted so that the output impedance of driver 46 matches the impedance of communication path 50 (FIG. 4). (See, e.g., page 32, lines 8-17 of applicants' specification.) If it is desired to make changes to the output voltage swing V_{OD}, the current source circuitry 78 and/or resistor circuitry 80 may be adjusted. (See, e.g., page 32, lines 3-7.)

The output of voltage source 86, which is labeled V_{CM} in FIG. 5, controls the common-mode voltage of the output driver. (See, e.g., page 31, line 22 to page 32, line 2.) It may be desirable to use the adjustable voltage source 86 to adjust V_{CM} to reduce mismatch between the common-mode voltage V_{CM} at output driver 46 and the common-mode voltage level being used at the corresponding input driver to which the output driver is transmitting data. (See, e.g., page 18, line 20 to page 19, line 1.)

Claim 2, which has been placed into independent form by incorporating the features of original claim 1, is directed to adjustable differential output driver circuitry having adjustable current source circuitry, adjustable resistor circuitry, and an adjustable voltage source that controls the common-mode voltage V_{CM}.

The Gabara patent, which was said to anticipate claim 2 under 35 U.S.C. 102(b), does not show or suggest the features of claim 2.

In FIG. 6 of the Gabara patent, Gabara discloses an output buffer 11 having current source 20 and current sink 22. Output buffer 11 also has an active on-chip resistance 101, which is connected across transmission lines 14 and 16. As described at column 9, lines 30-58 of Gabara, resistor 101 has transistors 102 and 104. According to Gabara, when the gates of transistors 102 and 104 are biased to V_{RES} as shown in FIG. 6, the resistance of resistor 101 is equal to R_{EXT}. This resistance can be used to improve the matching characteristics of the output buffer 11 to the transmission lines 14 and 16 . (See, e.g., column 9, lines 39-45 in Gabara.)

In Gabara's arrangement, transmission lines 14 and 16 convey data from output buffer 11 on a first integrated circuit (chip 1) to input buffer 12' on a second integrated circuit (chip 2). (See, e.g., FIG. 1A.) As shown in FIG. 2, the input

buffer 12' on chip 2 has a voltage-controlled resistor 18'. In the diagram of FIG. 6, the vertical dotted line and broken lines that run across the right-hand portion of transmission lines 14 and 16 indicate that resistor 18' is located on a separate integrated circuit from output driver 11.

As the circuit diagrams of FIGS. 1A, 2, and 6 make clear, resistor 18' is not part of Gabara's output buffer 11 and cannot be used to make any resistance, current, or voltage adjustments for Gabara's output buffer.

In the Office Action, it was suggested that Gabara's resistor 18' was the same as the adjustable resistor circuitry in applicants' claimed adjustable output driver circuitry. (Office Action, page 2.) It was also suggested that Gabara's resistor 101 was the same as applicants' claimed adjustable voltage source. (Office Action, page 3.) Applicants disagree.

Gabara's resistor 101 is described in Gabara at column 9, lines 30-58. As the circuit diagram of FIG. 6 and the discussion of column 9, lines 30-58 make clear, resistor 101 is not an adjustable voltage source that makes common mode voltage adjustments. Moreover, resistor 18' is not part of Gabara's output buffer 11, so resistor 18' cannot be equated with the adjustable resistor circuitry in applicants' claimed adjustable output driver circuitry.

Claim 2 is therefore not anticipated by Gabara and is in condition for allowance. Claim 4 depends from claim 2 and is allowable because claim 2 is allowable.

Claims 6-10 and 19-26

Claims 6-10 and 19-26 were indicated to be allowable.

Claims 11-18

Claim 11 is directed to an integrated circuit that has a dynamically adjustable differential output driver and dynamic control circuitry that controls the dynamically adjustable differential output driver. The dynamically adjustable differential output driver produces differential output data signals having a peak-to-peak output voltage swing V_{OD}. During operation, the dynamic control circuitry receives information from another integrated circuit to which the differential output data signals have been transmitted. Based on the information received from the other integrated circuit, the dynamic control circuitry controls the dynamically adjustable differential output driver dynamically in real time to adjust the peak-to-peak output voltage swing V_{OD}.

Nothing like the arrangement of claim 11 is shown or suggested in Gabara. As shown in FIG. 2 of Gabara, reference voltages V_{LOW} and V_{HIGH} serve as inputs to $V_{SOURCE/SINK}$ reference

circuit 45 in Gabara's output buffer 11. Reference circuit 45 uses the reference voltages V_{LOW} and V_{HIGH} in producing bias voltages V_{SOURCE} and V_{SINK} for biasing the transistors in current source 20 and current sink 22. As described at column 3, lines 36-41 in Gabara, the reference voltages V_{LOW} and V_{HIGH} "may be generated either externally or internally."

In the Office Action, it was suggested that the signals V_{LOW} and V_{HIGH} were received by Gabara's buffer 11 from chip 2 of FIG. 1B. Applicants disagree.

There is nothing in Gabara that shows or suggests transmitting any output buffer control signals from chip 2 to chip 1, let alone the signals V_{LOW} and V_{HIGH}. The only way in which data is passed from chip 2 to chip 1 in Gabara is through the use of transmission lines 14'/16' of FIG. 1B. However, Gabara makes no mention of using chip 2 to generate the V_{LOW} and V_{HIGH} signals for chip 1 or of using lines 14'/16' to provide the V_{LOW} and V_{HIGH} signals to chip 1. The voltages V_{LOW} and V_{HIGH} are reference signals that are used with the circuitry of reference circuit 45 to compensate output buffer 11 for variations in process, voltage, and temperature, they are not conveyed from chip 2 to chip 1.

Because claim 11 is directed toward an integrated circuit with dynamic control circuitry that controls an adjustable differential output driver based on information

received from another integrated circuit, whereas Gabara does not show or suggest that chip 2 provides any such information to chip 1, claim 11 is not anticipated by Gabara. Claim 11 is therefore allowable. Claims 12-18 depend from claim 11 and are allowable because claim 11 is allowable.

Claims 27-32

Claim 27 is directed toward a method for controlling a differential output driver at a first integrated circuit using information received from a second integrated circuit.

Method claim 27 is allowable over Gabara at least for the reasons that apparatus claim 11 is allowable over Gabara. In Gabara's approach, chip 2 does not provide information to chip 1 that chip 1 uses to control a differential output driver. The signals V_{LOW} and V_{HIGH} that the Office Action suggested were sent to chip 1 from chip 2 are not generated by chip 2.

Claim 27 is therefore not anticipated by Gabara and is in condition for allowance. Claims 28-32 depend from claim 27 and are allowable because claim 27 is allowable.

Conclusion

The foregoing demonstrates that claims 1, 2, 4, and 6-32 are patentable. This application is therefore in condition

for allowance. Reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,

G. Victor Treyz 4/7/05

G. Victor Treyz
Reg. No. 36,294
Attorney for Applicants
Customer No. 45851